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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,758	09/15/2001	Chikashi Okamoto	ASA-1003	2349

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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/856,758	OKAMOTO ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,13 and 14* is/are rejected.

7)☒ Claim(s) *5,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1, 2, 5, 11 and 14 are objected to because of the following informalities:

In Claim 1, lines 3, 10 and 13: "planer" should be changed to --planar--.

In Claim 2, line 4: "circuits" should be changed to --circuit--.

In Claim 5, lines 1, 10 and 18: "planer" should be changed to --planar--.

In Claim 5, line 4: "in that" should be deleted and replaced with --by--.

In Claim 5, lines 6-7, the following changes should be made:

"...than a size of each of the rectangular areas which are obtained by sectioning the sheet surface..."

In Claim 11, line 10: "the" should be changed to --a--.

In Claim 11, line 14: "a" should be changed to --the--.

In Claim 11, line 21: "a" should be changed to --the--.

In Claim 14, line 14: "with" should be changed to --within--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Claim 13 recites the limitation "the another electric element" in lines 8-9, 10-11 and 14-15. There is insufficient antecedent basis for this limitation in the claim. Perhaps the Applicant intended to replace "the another electric element" with --the capacitor--. Amending the claim thusly would overcome the rejection.

b) Claim 14, lines 9-12, recite "the capacitor, the electronic circuit chip and the antenna are mounted on the sheet so that **the planar surface of the capacitor and the planar surface of the capacitor** are in parallel with the sheet surface" (bold and underlined emphasis by the Examiner). The above bold-highlighted phrase repeats "the capacitor" twice; obviously, the Applicant contemplated one or more of the other claimed components in one of the two positions in the above-cited excerpt occupied by "the capacitor." The Applicant must amend the above excerpt to recite the appropriate component(s) in order to overcome the rejection.

c) Claim 14 recites the limitation "the electronic circuit part" in line 17. There is insufficient antecedent basis for this limitation in the claim. This rejection may be overcome by changing "part" to --chip-- in line 17.

Rejections Based On Prior Art

4. The following references were relied upon for the rejections hereinbelow:

Yamaguchi et al. (US 6,147,876)	Scott (US 6,118,072)
Ingraham et al. (US 6,061,245)	Gustafson (US 6,050,622)
Denney, Jr. et al. (US 5,818,692)	Tessier et al. (US 5,789,815)
Takamiya (JP01-122982 U)*	Goff et al. (US 6,154,137)

Usami et al. (US 5,689,136)

*Submitted by Applicant with IDS filed on May 25, 2001.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al.

Yamaguchi et al. discloses, in Figs. 7 and 30: A method of mounting a planar electronic circuit chip 201 (Fig. 7) on a flexible sheet F (Fig. 30) together with another planar electric element (PWB 100 of module 5A; Figs. 7 and 30), characterized by steps of: selecting the another electric element 100 and the electronic circuit chip 201 so that

the planar surface of the another electric element 100 is greater than the planar surface of the electronic circuit chip 201 (Fig. 7); and mounting the another electric element 100 and the electronic circuit chip 201 (together forming module 5A) onto the sheet F (Fig. 30) so that the planar surface of the another electronic element 100 and the planar surface of the electronic circuit chip 201 are located in parallel with the surface of the sheet (Fig. 30), and the planar surface of the electronic circuit chip 201 is accommodated within the planar surface of the another electric element 100 as viewed in a direction perpendicular to the surface of the sheet (Figs. 7 and 30).

7. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Denney, Jr. et al.

Denney, Jr. et al. discloses, in Figs. 2 and 3: A method of mounting a circuit chip (col.3: 21-29) on a foldable sheet 18 having a rectangular sheet surface 22 (col.3: 37-41), characterized in that the electronic circuit chip 10 is mounted on the sheet 18 so as to prevent the electronic circuit chip from being located at least at a position which is obtained by 1/3 of the length of longer sides of the sheet surface 22 and by ½ of the length of short sides of the sheet surface 22.

8. Claims 2, 4 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Takamiya.

As to Claim 2, Takamiya (JP01-122982 U) discloses: A method of mounting an electronic circuit chip 5 onto a foldable sheet 1 (Fig. 2), characterized in that the electronic circuit chip 5 is mounted to the sheet 1 so that the electronic circuit chip 5 is

prevented from being located at a position where a crease 2 is formed when the sheet is folded (Fig. 3).

As to Claim 4, Takamiya further discloses, in Fig. 2, that electronic circuit chip 5 is mounted at a position in the vicinity of an edge of the sheet surface.

As to Claim 8, Takamiya further discloses, in Figs. 1-3 that sheet 1 is tape-like (i.e., is flexible and can be folded).

9. Claims 2, 4 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Tessier et al.

As to Claim 2, Tessier et al. discloses: A method of mounting an electronic circuit chip 30 onto a foldable sheet 26 (Fig. 1; col.2: 17-20), characterized in that the electronic circuit chip 30 is mounted to the sheet 26 so that the electronic circuit chip 30 is prevented from being located at a position where a crease is formed when the sheet is folded (Fig. 5).

As to Claim 4, Tessier et al. further discloses, in Fig. 1, that electronic circuit chip 30 is mounted at a position in the vicinity of an edge of the sheet surface.

As to Claim 8, Tessier et al. further discloses that sheet 26 is tape-like (col.3: 66-col.4: 3; col.4: 13-15).

10. Claims 2. 4. 6 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ingraham et al.

As to Claim 2, Ingraham et al. discloses, in Fig. 1A: A method of mounting an electronic circuit chip 123 onto a foldable sheet 101, characterized in that the electronic circuit chip 123 is mounted to the sheet 101 so that the electronic circuit chip 123 is

prevented from being located at a position where a crease is formed when the sheet 1 is folded.

As to Claim 4, Ingraham et al. further discloses, in Fig. 1A, that electronic circuit chip 123 is mounted at a position in the vicinity of an edge of the sheet surface.

As to Claim 6, Ingraham et al. further discloses that a long rod-like electric part 111 is mounted on the sheet 101 so that the longitudinal direction of the electric part is coincident with the sidewise direction of the sheet (Fig. 1A; col.3: 5-13 and 28-31).

As to Claim 8, Ingraham et al. further discloses that sheet 101 is tape-like (i.e., is flexible and can be folded; col.1: 57-60).

11. Claims 2, 4, 7, 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Gustafson.

As to Claim 2, Gustafson discloses, in Figs. 1 and 2: A method of mounting an electronic circuit chip 20 (col.3: 38-45) onto a foldable sheet 1, characterized in that the electronic circuit chip 20 is mounted to the sheet 1 so that the electronic circuit chip 20 is prevented from being located at a position where a crease is formed when sheet 1 is folded.

As to Claim 4, Gustafson further discloses that the electronic circuit chip 20 is mounted at a position in the vicinity of an edge of the sheet surface (Figs. 1 and 2).

As to Claim 7, Gustafson further discloses that sheet 1 is made of paper (col.3: 14-15; col.6: 58-63).

As to Claim 8, Gustafson further discloses, in Figs. 1 and 2, that sheet 1 is tape-like (i.e., is flexible and can be folded).

As to Claim 10, Gustafson further discloses that electronic circuit chip 20 is mounted on the surface of one of two front and rear sheet surfaces of sheet 1 (through adhesive 14 (Figs. 1 and 5).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takamiya in view of Scott.

I. Takamiya discloses a foldable sheet of flexible material but does not teach that the material is paper.

II. Scott discloses a foldable, flexible chip-carrying sheet 22 (Fig. 3) that can be made of material selected from among various plastics and paper (col.4: 63-col.5: 3).

III. Since both Takamiya and Scott are both in the art of electronics packaging requiring foldable, flexible sheets as circuit substrates, then the use of paper, as taught by Scott, would have been readily recognized as useful in the pertinent art of Takamiya in order to meet performance and cost requirements for applications in which a paper sheet would be more suitable than other art-recognized equivalent materials taught by Scott.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the flexible sheet of Takamiya using paper, as taught by Scott, in order to form the foldable circuit substrate with the required physical and electrical performance for the application.

14. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tessier et al in view of Scott.

I. Tessier et al. discloses a foldable, flexible polyimide sheet 26 (col.3: 66-col.4: 3; col.4: 13-15 and 20-23) but does not teach the use of a paper material for sheet 26.

II. Scott discloses a foldable, flexible chip-carrying sheet 22 (Fig. 3) that can be made of material selected from among various plastics (e.g., polyimide) and paper (col.4: 63-col.5: 3).

III. Since both Tessier et al. and Scott are both in the art of electronics packaging requiring foldable, flexible sheets as circuit substrates, then the use of paper, as taught by Scott, would have been readily recognized as useful in the pertinent art of Tessier et al. in order to meet performance and cost requirements in applications for which a paper sheet would be more suitable than the other art-recognized equivalent materials taught by Scott.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the flexible sheet of Tessier et al. using the art-recognized equivalent paper instead of polyimide, as taught by Scott, in order to form the foldable circuit substrate with the required physical and electrical performance for the application.

15. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ingraham et al. in view of Scott.

I. Ingraham et al. discloses a foldable, flexible sheet 101 made of polyimide (col.1: 57-60) but does not teach the use of paper material for sheet 101.

II. Scott discloses a foldable, flexible chip-carrying sheet 22 that can be made of material selected from among various plastics (e.g., polyimide) and paper (col.4: 63-col.5: 3).

III. Since both Ingraham et al. and Scott are both in the art of electronics packaging requiring foldable, flexible sheets as circuit substrates, then the use of paper, as taught by Scott, would have been readily recognized as useful in the pertinent art of Ingraham et al. in order to meet performance and cost requirements in applications for which a paper sheet would be more suitable than the other art-recognized equivalent materials taught by Scott.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the flexible sheet of Ingraham et al. using the art-recognized equivalent paper instead of polyimide, as taught by Scott, in order to form the foldable circuit substrate with the required physical and electrical performance for the application.

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over **each** of Takamiya, Tessier et al. and Ingraham et al. in view of Scott, as applied to Claim 7 above, and further in view of Usami et al.

I. **Each** of Takamiya, Tessier et al. and Ingraham et al. has been modified by Scott such that the sheet material is made of paper, as taught by Scott. However, **each** of Takamiya, Tessier et al. and Ingraham et al., as modified by Scott, do not teach that the sheet has a two layer structure wherein the electronic circuit chip is mounted between two layers of the sheet.

II. Usami et al. discloses a sheet having a two layer structure comprising plastic materials 36′ and 36″ that embeds IC chip 35 (Figs. 17 and 18; col.9: 14-22) so that the chip lies in a neutral plane 37 in order to protect chip 35 from the bending forces when the sheet is bent or flexed (Fig. 19).

III. Since **each** of Takamiya, Tessier et al. and Ingraham et al. disclose sheets that are foldable, flexible and, as modified by Scott, made of paper, and furthermore, having an electronic chip mounted thereon, then the further modification of a two layer sheet structure embedding the chip for the purpose of protecting the chip from the bending forces when the sheet is flexed, as taught by Usami et al., would have been readily recognized in the pertinent art of Takamiya, Tessier et al. and Ingraham et al., respectively, as modified by Scott.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify **each** of Takamiya, Tessier et al. and Ingraham et al., as modified by Scott, by providing the two layer sheet structure in order to protect the chips mounted on the sheet from damage or electrical disconnection due to the bending forces under flexure, as taught by Usami et al.

17. Claim 13 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection, above) is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Goff et al.

I. Yamaguchi et al. discloses, in Figs. 7, 23, 24 and 30: A foldable sheet F having a rectangular sheet surface and mounted thereon with an electric circuit 5A or 5D (Figs. 7, 24 and 30) composed of a planar electric circuit chip (201 in Fig. 7 and 201D in Fig. 24), a planar capacitor (capacitors 122 in Fig. 23 and 137 in Fig. 24; col.13: 5-10; col.14: 6-9 and 40-42), characterized in that chip 201 is mounted on sheet F so that it is prevented from being located at a position where a crease is created when sheet F is folded in a predetermined folding method, and the [sic] another electric element (PWB 100D of electric circuit 5A in Fig. 24) and chip 201D are mounted on sheet F so that the planar surface of the another electric element 100D and the planar surface of the chip 201D are in parallel with the surface of sheet F (Figs. 24 and 30); the planar surface of chip 201D (Fig. 24) or 201 (Fig. 7) is accommodated within the planar surface of the another electric element 100D (Fig. 24) or 100 (Fig. 7), as viewed in a direction perpendicular to the surface of the sheet F (Figs. 7, 24 and 30).

II. Yamaguchi et al. does not teach an antenna mounted on sheet F so that the longitudinal direction of the antenna is coincident with the sidewise direction of sheet F.

III. Goff et al. discloses an ID tag substrate 111 on which an IC 12 and a dipole antenna 14 (or 23) is mounted (Figs. 1A, 5 and 6) and wherein the longitudinal direction of the dipole antenna is coincident with the sidewise direction of ID tag substrate 111.

Also, Goff et al. includes a capacitor 16 (see embodiment of Fig. 8) in order to enhance the performance of the ID tag (col.5: 46-col.6: 4).

IV. Since Yamaguchi et al. and Goff et al. both teach electric circuits with planar active and passive devices mounted thereon, then the inclusion of an antenna in the electric circuit of Yamaguchi et al. situated such that its longitudinal direction coincides with the direction of the circuit substrate and/or sheet, as taught by Goff et al., would have been readily recognized in the pertinent art of Yamaguchi et al. in order to meet the requirements of a communications electronics application of the electric circuit, as taught by Goff et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the electric circuit of Yamaguchi et al. a dipole antenna mounted on the sheet so that the longitudinal direction of the antenna is coincident with the sidewise direction of sheet F, as taught by Goff et al., in order to enhance the functionality of the electric circuit of Yamaguchi et al. and thereby meet the requirements of a communications electronics application, such as an ID tag, as taught by Goff et al.

Allowable Subject Matter

18. Claims 5 and 11-12 would be allowable if rewritten or amended to overcome the objection(s) set forth in this Office action.

19. Claim 14 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

20. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 5, patentability resides in **the combination of** *setting the planar surface of the another electric element to be slightly smaller than a size of each of the rectangular areas which are obtained by sectioning the sheet surface by n x m (where n and m are integers larger than 2)* **and** *wherein the planar surface of the another electric element is accommodated within one of the rectangular areas, as viewed in a direction perpendicular to the sheet surface*, in combination with the other limitations of the claim.

As to Claims 11-12, patentability resides in *the claimed dimensional and mechanical properties of the electronic circuit chip defined by* $3PL^2 + 6WL + \sigma H^2 \leq 0$, in combination with the other limitations of base Claim 11.

As to Claim 14, given the indeterminate scope of the claim as indicated in the 35 USC § 112, 2nd paragraph rejection of Claim 14, above, patentability appears to reside in the limitation wherein *the planar surface of the electronic circuit chip and the contour of the antenna are accommodated within the planar surface of the capacitor as viewed in a direction perpendicular to the sheet surface*, *provisionally* in combination with the other limitations of the claim.

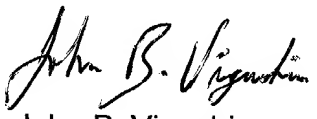
21. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Examiner
Art Unit 2827

jbv
March 15, 2003